



**256K X 36, 512K X 18**  
**3.3V Synchronous SRAMs**  
**3.3V I/O, Burst Counter**  
**Pipelined Outputs, Single Cycle Deselect**

**AS8C803600**  
**AS8C801800**

**Features**

- ◆ 256K x 36, 512K x 18 memory configurations
- ◆ Supports high system speed:
  - 150MHz 3.8ns clock access time
- ◆  $\overline{\text{LBO}}$  input selects interleaved or linear burst mode
- ◆ Self-timed write cycle with global write control ( $\overline{\text{GW}}$ ), byte write enable ( $\overline{\text{BWE}}$ ), and byte writes ( $\overline{\text{BWx}}$ )
- ◆ 3.3V core power supply
- ◆ Power down controlled by ZZ input
- ◆ 3.3V I/O supply ( $\text{VDDO}$ )
- ◆ Packaged in a JEDEC Standard 100-pin thin plastic quad flatpack (TQFP)

256K x 36 / 512K x 18. The SRAMs contain write, data, address and control registers. Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the AS8C803600/801800 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will be pipelined for one cycle before it is available on the next rising clock edge. If burst mode operation is selected ( $\overline{\text{ADV}}=\text{LOW}$ ), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses are defined by the internal burst counter and the  $\overline{\text{LBO}}$  input pin.

The AS8C803600/801800 SRAMs utilize the latest high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP).

**Description**

The AS8C803600/801800 are high-speed SRAMs organized as

**Pin Description Summary**

A0-A18	Address Inputs	Input	Synchronous
$\overline{\text{CE}}$	Chip Enable	Input	Synchronous
CS0, $\overline{\text{CS}}_1$	Chip Selects	Input	Synchronous
$\overline{\text{OE}}$	Output Enable	Input	Asynchronous
$\overline{\text{GW}}$	Global Write Enable	Input	Synchronous
$\overline{\text{BWE}}$	Byte Write Enable	Input	Synchronous
$\overline{\text{BW}}_1, \overline{\text{BW}}_2, \overline{\text{BW}}_3, \overline{\text{BW}}_4^{(1)}$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$\overline{\text{ADV}}$	Burst Address Advance	Input	Synchronous
$\overline{\text{ADSC}}$	Address Status (Cache Controller)	Input	Synchronous
$\overline{\text{ADSP}}$	Address Status (Processor)	Input	Synchronous
$\overline{\text{LBO}}$	Linear / Interleaved Burst Order	Input	DC
ZZ	Sleep Mode	Input	Asynchronous
I/O0-I/O31, I/OP1-I/OP4	Data Input / Output	I/O	Synchronous
VDD, VDDO	Core Power, I/O Power	Supply	N/A
VSS	Ground	Supply	N/A

NOTE:

1.  $\overline{\text{BW}}_3$  and  $\overline{\text{BW}}_4$  are not applicable for other devices

5310 tbl 01

## Pin Definitions<sup>(1)</sup>

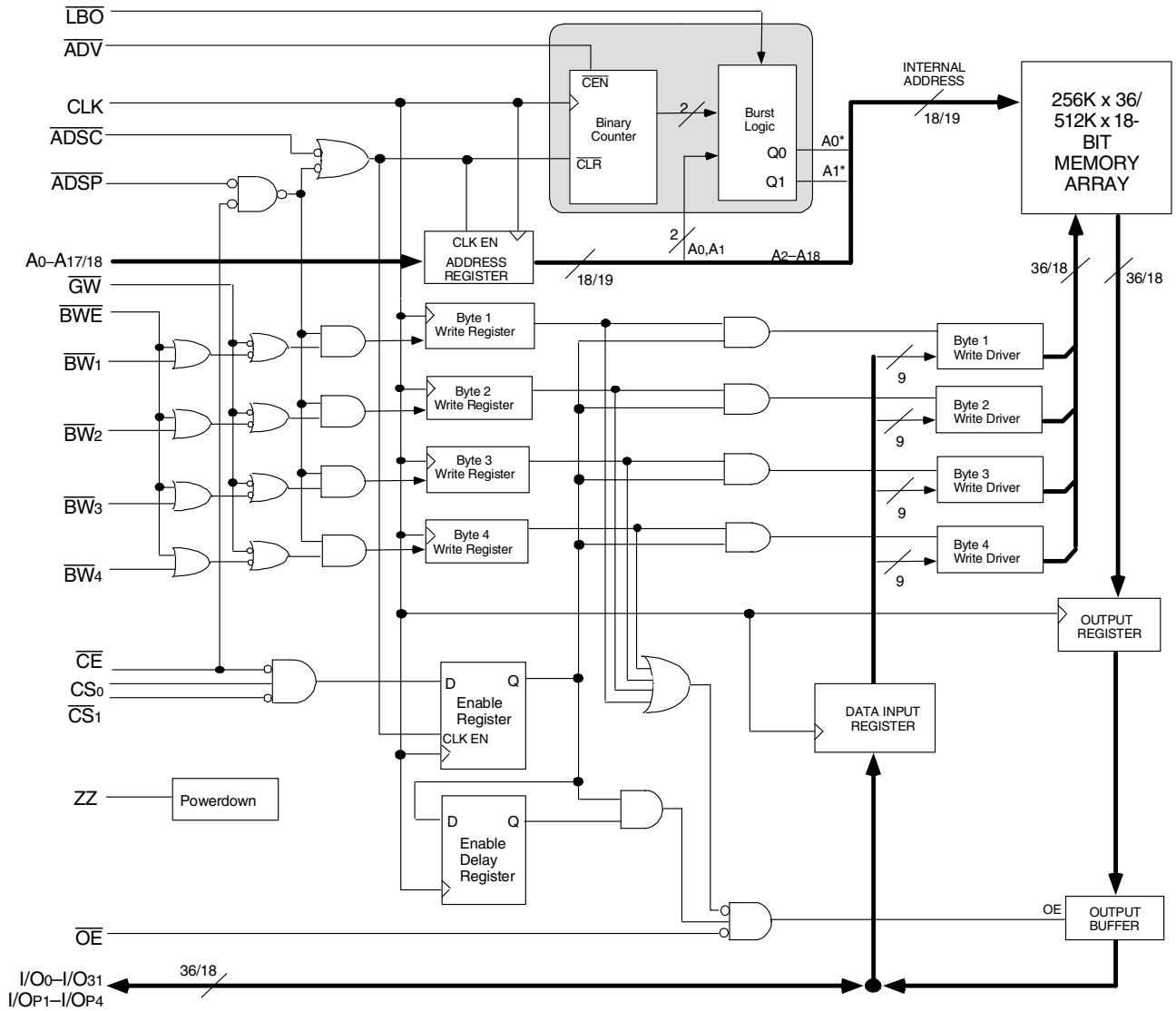
Symbol	Pin Function	I/O	Active	Description
A0-A18	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and $\overline{\text{ADSC}}$ Low or $\overline{\text{ADSP}}$ Low and $\overline{\text{CE}}$ Low.
$\overline{\text{ADSC}}$	Address Status (Cache Controller)	I	LOW	Synchronous Address Status from Cache Controller. $\overline{\text{ADSC}}$ is an active LOW input that is used to load the address registers with new addresses.
$\overline{\text{ADSP}}$	Address Status (Processor)	I	LOW	Synchronous Address Status from Processor. $\overline{\text{ADSP}}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{\text{ADSP}}$ is gated by $\overline{\text{CE}}$ .
$\overline{\text{ADV}}$	Burst Address Advance	I	LOW	Synchronous Address Advance. $\overline{\text{ADV}}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When the input is HIGH the burst counter is not incremented; that is, there is no address advance.
$\overline{\text{BWE}}$	Byte Write Enable	I	LOW	Synchronous byte write enable gates the byte write inputs $\overline{\text{BW1}}\text{-}\overline{\text{BW4}}$ . If $\overline{\text{BWE}}$ is LOW at the rising edge of CLK then $\overline{\text{BWx}}$ inputs are passed to the next stage in the circuit. If $\overline{\text{BWE}}$ is HIGH then the byte write inputs are blocked and only $\overline{\text{GW}}$ can initiate a write cycle.
$\overline{\text{BW1}}\text{-}\overline{\text{BW4}}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. $\overline{\text{BW1}}$ controls I/O0-7, I/OP1, $\overline{\text{BW2}}$ controls I/O8-15, I/OP2, etc. Any active byte write causes all outputs to be disabled.
$\overline{\text{CE}}$	Chip Enable	I	LOW	Synchronous chip enable. $\overline{\text{CE}}$ is used with $\text{CS0}$ and $\overline{\text{CS1}}$ to enable the IDT71V67603/7803. $\overline{\text{CE}}$ also gates $\overline{\text{ADSP}}$ .
CLK	Clock	I	N/A	This is the clock input. All timing references for the device are made with respect to this input.
$\text{CS0}$	Chip Select 0	I	HIGH	Synchronous active HIGH chip select. $\text{CS0}$ is used with $\overline{\text{CE}}$ and $\overline{\text{CS1}}$ to enable the chip.
$\overline{\text{CS1}}$	Chip Select 1	I	LOW	Synchronous active LOW chip select. $\overline{\text{CS1}}$ is used with $\overline{\text{CE}}$ and $\text{CS0}$ to enable the chip.
$\overline{\text{GW}}$	Global Write Enable	I	LOW	Synchronous global write enable. This input will write all four 9-bit data bytes when LOW on the rising edge of CLK. $\overline{\text{GW}}$ supersedes individual byte write enables.
I/O0-I/O31 I/OP1-I/OP4	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
$\overline{\text{LBO}}$	Linear Burst Order	I	LOW	Asynchronous burst order selection input. When $\overline{\text{LBO}}$ is HIGH, the interleaved burst sequence is selected. When $\overline{\text{LBO}}$ is LOW the Linear burst sequence is selected. $\overline{\text{LBO}}$ is a static input and must not change state while the device is operating.
$\overline{\text{OE}}$	Output Enable	I	LOW	Asynchronous output enable. When $\overline{\text{OE}}$ is LOW the data output drivers are enabled on the I/O pins if the chip is also selected. When $\overline{\text{OE}}$ is HIGH the I/O pins are in a high-impedance state.
VDD	Power Supply	N/A	N/A	3.3V core power supply.
VDDO	Power Supply	N/A	N/A	3.3V I/O Supply.
VSS	Ground	N/A	N/A	Ground.
NC	No Connect	N/A	N/A	NC pins are not electrically connected to the device.
ZZ	Sleep Mode	I	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the AS8C803600/1800 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.

**NOTE:**

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

5310 tbl 02

### Functional Block Diagram



5301 drw 01

### Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Commercial	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V <sub>TERM</sub> <sup>(3,6)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>DD</sub>	V
V <sub>TERM</sub> <sup>(4,6)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>DD</sub> +0.5	V
V <sub>TERM</sub> <sup>(5,6)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>DDQ</sub> +0.5	V
T <sub>A</sub> <sup>(7)</sup>	Operating Temperature	-0 to +70	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
P <sub>T</sub>	Power Dissipation	2.0	W
I <sub>OUT</sub>	DC Output Current	50	mA

**NOTES:**

5310 tbl 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>DD</sub> terminals only.
- V<sub>DDQ</sub> terminals only.
- Input terminals only.
- I/O terminals only.
- This is a steady-state DC parameter that applies after the power supplies have ramped up. Power supply sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V<sub>DDQ</sub> during power supply ramp up.
- T<sub>A</sub> is the "instant on" case temperature.

### Recommended Operating Temperature and Supply Voltage

Grade	Temperature <sup>(1)</sup>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0°C to +70°C	0V	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	3.3V±5%

**NOTE:**

5310 tbl 04

- T<sub>A</sub> is the "instant on" case temperature.

### Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage	3.135	3.3	3.465	V
V <sub>DDQ</sub>	I/O Supply Voltage	3.135	3.3	3.465	V
V <sub>SS</sub>	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage - Inputs	2.0	—	V <sub>DD</sub> +0.3	V
V <sub>IH</sub>	Input High Voltage - I/O	2.0	—	V <sub>DDQ</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.8	V

5310 tbl 05

**NOTE:**

- V<sub>IL</sub> (min) = -1.0V for pulse width less than t<sub>CVZ</sub>/2, once per cycle.

### 100 Pin TQFP Capacitance (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	5	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 3dV	7	pF

5310 tbl 07

### 165 fBGA Capacitance (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	7	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 3dV	7	pF

5310 tbl 07b

### 119 BGA Capacitance (T<sub>A</sub> = +25°C, f = 1.0MHz)

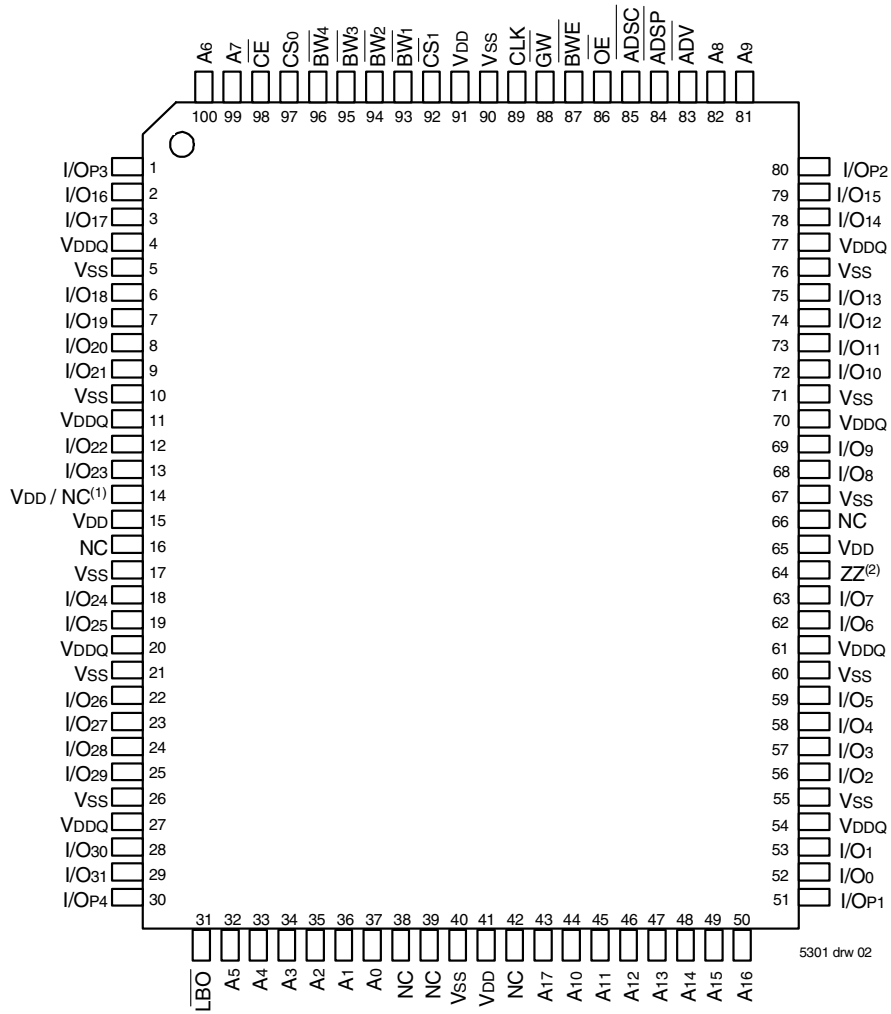
Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	7	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 3dV	7	pF

5310 tbl 07a

**NOTE:**

- This parameter is guaranteed by device characterization, but not production tested.

## Pin Configuration – 256K x 36, 100-Pin TQFP

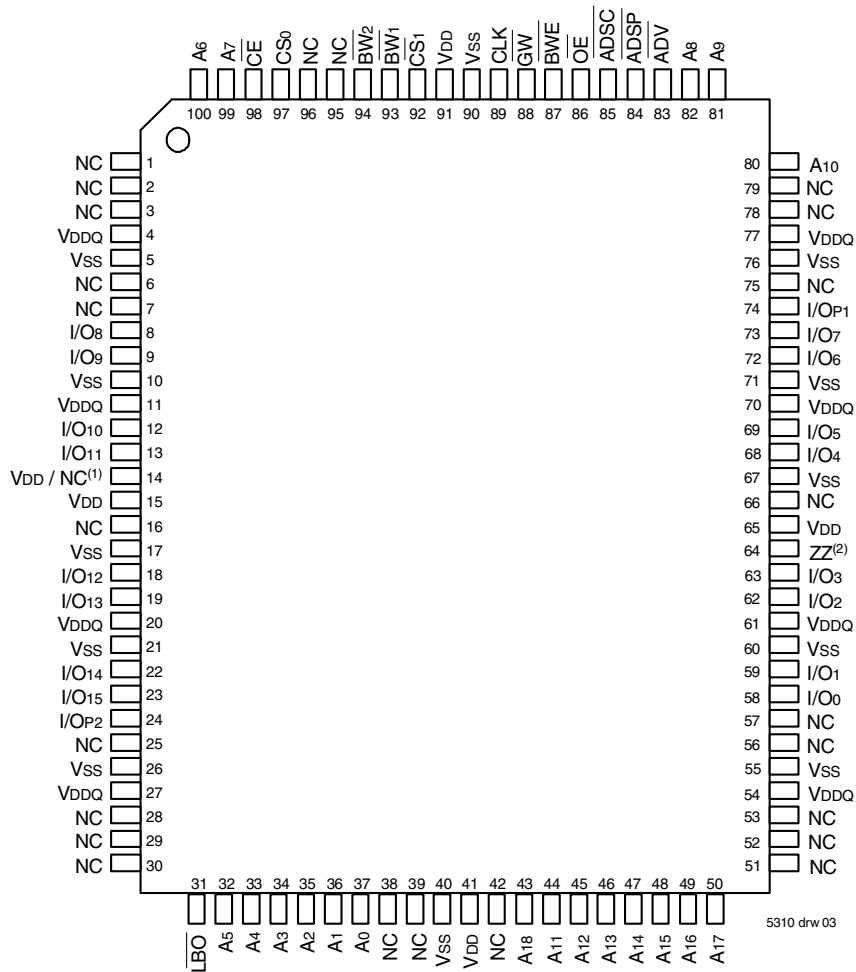


### Top View

**NOTES:**

1. Pin 14 can either be directly connected to VDD, or connected to an input voltage  $\geq V_{IH}$ , or left unconnected.
2. Pin 64 can be left unconnected and the device will always remain in active mode.

# Pin Configuration – 512K x 18, 100-Pin QFP



## Top View

**NOTES:**

1. Pin 14 can either be directly connected to VDD, or connected to an input voltage  $\geq V_{IH}$ , or left unconnected.
2. Pin 64 can be left unconnected and the device will always remain in active mode.

### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ( $V_{DD} = 3.3V \pm 5\%$ )

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$ I_{L1} $	Input Leakage Current	$V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$	—	5	$\mu A$
$ I_{LZZ} $	ZZ and $\overline{LBO}$ Input Leakage Current <sup>(1)</sup>	$V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$	—	30	$\mu A$
$ I_{LO} $	Output Leakage Current	$V_{OUT} = 0V \text{ to } V_{DDQ}$ , Device Deselected	—	5	$\mu A$
$V_{OL}$	Output Low Voltage	$I_{OL} = +8mA, V_{DD} = \text{Min.}$	—	0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -8mA, V_{DD} = \text{Min.}$	2.4	—	V

5310 tbl 08

**NOTE:**

1. The  $\overline{LBO}$  pin will be internally pulled to  $V_{DD}$  if it is not actively driven in the application and the ZZ pin will be internally pulled to  $V_{SS}$  if not actively driven.

### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(1)</sup>

Symbol	Parameter	Test Conditions	166MHz	150MHz		133MHz		Unit
			Com'l only	Com'l	Ind	Com'l	Ind	
$I_{DD}$	Operating Power Supply Current	Device Selected, Outputs Open, $V_{DD} = \text{Max.}, V_{DDQ} = \text{Max.}, V_{IN} \geq V_{IH} \text{ or } \leq V_{IL}, f = f_{MAX}^{(2)}$	340	305	325	260	280	mA
$I_{SB1}$	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{DDQ} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = 0^{(2,3)}$	50	50	70	50	70	mA
$I_{SB2}$	Clock Running Power Supply Current	Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{DDQ} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = f_{MAX}^{(2,3)}$	160	155	175	150	170	mA
$I_{ZZ}$	Full Sleep Mode Supply Current	$ZZ \geq V_{HD}, V_{DD} = \text{Max.}$	50	50	70	50	70	mA

5310 tbl 09

**NOTES:**

- All values are maximum guaranteed values.
- At  $f = f_{MAX}$ , inputs are cycling at the maximum frequency of read cycles of  $1/t_{cvc}$  while  $\overline{ADSC} = \text{LOW}$ ;  $f=0$  means no input lines are changing.
- For I/Os  $V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V$ . For other inputs  $V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V$ .

### AC Test Conditions ( $V_{DDQ} = 3.3V$ )

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figure 1

5310 tbl 10

### AC Test Load

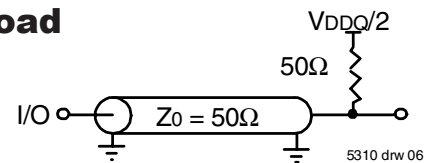


Figure 1. AC Test Load

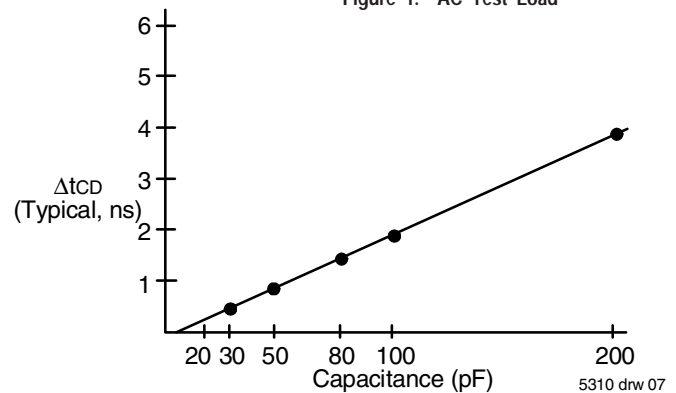


Figure 2. Lumped Capacitive Load, Typical Derating

### Synchronous Truth Table<sup>(1,3)</sup>

Operation	Address Used	$\overline{CE}$	CS <sub>0</sub>	$\overline{CS}_1$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_x$	$\overline{OE}$ (2)	CLK	I/O
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	X	H	L	X	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	L	X	L	X	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	X	H	X	L	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	L	X	X	L	X	X	X	X	X	-	HI-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	L	-	DOUT
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	H	-	HI-Z
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	H	X	L	-	DOUT
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	L	-	DOUT
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	H	-	HI-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	L	X	-	DIN
Write Cycle, Begin Burst	External	L	H	L	H	L	X	L	X	X	X	-	DIN
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	L	-	DOUT
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	H	-	HI-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	L	-	DOUT
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	H	-	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	L	-	DOUT
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	H	-	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	L	-	DOUT
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	H	-	HI-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L	X	-	DIN
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	X	X	-	DIN
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L	X	-	DIN
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	X	X	-	DIN
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	L	-	DOUT
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	H	-	HI-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	L	-	DOUT
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	H	-	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	L	-	DOUT
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	-	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	L	-	DOUT
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	H	-	HI-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L	X	-	DIN
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	X	X	-	DIN
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L	X	-	DIN
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	X	X	-	DIN

**NOTES:**

1. L = V<sub>IL</sub>, H = V<sub>IH</sub>, X = Don't Care.
2.  $\overline{OE}$  is an asynchronous input.
3. ZZ = low for this table.

5310 tbl 11



### Synchronous Write Function Truth Table<sup>(1, 2)</sup>

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$	$\overline{BW}_4$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all Bytes	L	X	X	X	X	X
Write all Bytes	H	L	L	L	L	L
Write Byte 1 <sup>(3)</sup>	H	L	L	H	H	H
Write Byte 2 <sup>(3)</sup>	H	L	H	L	H	H
Write Byte 3 <sup>(3)</sup>	H	L	H	H	L	H
Write Byte 4 <sup>(3)</sup>	H	L	H	H	H	L

5310 tbl 12

**NOTES:**

1. L =  $V_{IL}$ , H =  $V_{IH}$ , X = Don't Care.
2.  $\overline{BW}_3$  and  $\overline{BW}_4$  are not applicable other devices
3. Multiple bytes may be selected during the same cycle.

### Asynchronous Truth Table<sup>(1)</sup>

Operation <sup>(2)</sup>	$\overline{OE}$	ZZ	I/O Status	Power
Read	L	L	Data Out	Active
Read	H	L	High-Z	Active
Write	X	L	High-Z - Data In	Active
Deselected	X	L	High-Z	Standby
Sleep Mode	X	H	High-Z	Sleep

5310 tbl 13

**NOTES:**

1. L =  $V_{IL}$ , H =  $V_{IH}$ , X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

### Interleaved Burst Sequence Table ( $\overline{LBO}=V_{DD}$ )

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address <sup>(1)</sup>	1	1	1	0	0	1	0	0

5310 tbl 14

**NOTE:**

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

### Linear Burst Sequence Table ( $\overline{LBO}=V_{SS}$ )

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address <sup>(1)</sup>	1	1	0	0	0	1	1	0

5310 tbl 15

**NOTE:**

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

## AC Electrical Characteristics

(VDD = 3.3V ±5%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	166MHz		150MHz		133MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>CYC</sub>	Clock Cycle Time	6	—	6.7	—	7.5	—	ns
t <sub>CH</sub> <sup>(1)</sup>	Clock High Pulse Width	2.4	—	2.6	—	3	—	ns
t <sub>CL</sub> <sup>(1)</sup>	Clock Low Pulse Width	2.4	—	2.6	—	3	—	ns
<b>Output Parameters</b>								
t <sub>CD</sub>	Clock High to Valid Data	—	3.5	—	3.8	—	4.2	ns
t <sub>DC</sub>	Clock High to Data Change	1.5	—	1.5	—	1.5	—	ns
t <sub>CLZ</sub> <sup>(2)</sup>	Clock High to Output Active	0	—	0	—	0	—	ns
t <sub>CHZ</sub> <sup>(2)</sup>	Clock High to Data High-Z	1.5	3.5	1.5	3.8	1.5	4.2	ns
t <sub>OE</sub>	Output Enable Access Time	—	3.5	—	3.8	—	4.2	ns
t <sub>OLZ</sub> <sup>(2)</sup>	Output Enable Low to Output Active	0	—	0	—	0	—	ns
t <sub>OHZ</sub> <sup>(2)</sup>	Output Enable High to Output High-Z	—	3.5	—	3.8	—	4.2	ns
<b>Set Up Times</b>								
t <sub>SA</sub>	Address Setup Time	1.5	—	1.5	—	1.5	—	ns
t <sub>SS</sub>	Address Status Setup Time	1.5	—	1.5	—	1.5	—	ns
t <sub>SD</sub>	Data In Setup Time	1.5	—	1.5	—	1.5	—	ns
t <sub>SW</sub>	Write Setup Time	1.5	—	1.5	—	1.5	—	ns
t <sub>SAV</sub>	Address Advance Setup Time	1.5	—	1.5	—	1.5	—	ns
t <sub>SC</sub>	Chip Enable/Select Setup Time	1.5	—	1.5	—	1.5	—	ns
<b>Hold Times</b>								
t <sub>HA</sub>	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>HS</sub>	Address Status Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>HD</sub>	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>HW</sub>	Write Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>HAV</sub>	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>HC</sub>	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	ns
<b>Sleep Mode and Configuration Parameters</b>								
t <sub>ZZPW</sub>	ZZ Pulse Width	100	—	100	—	100	—	ns
t <sub>ZZR</sub> <sup>(3)</sup>	ZZ Recovery Time	100	—	100	—	100	—	ns
t <sub>CFG</sub> <sup>(4)</sup>	Configuration Set-up Time	24	—	27	—	30	—	ns

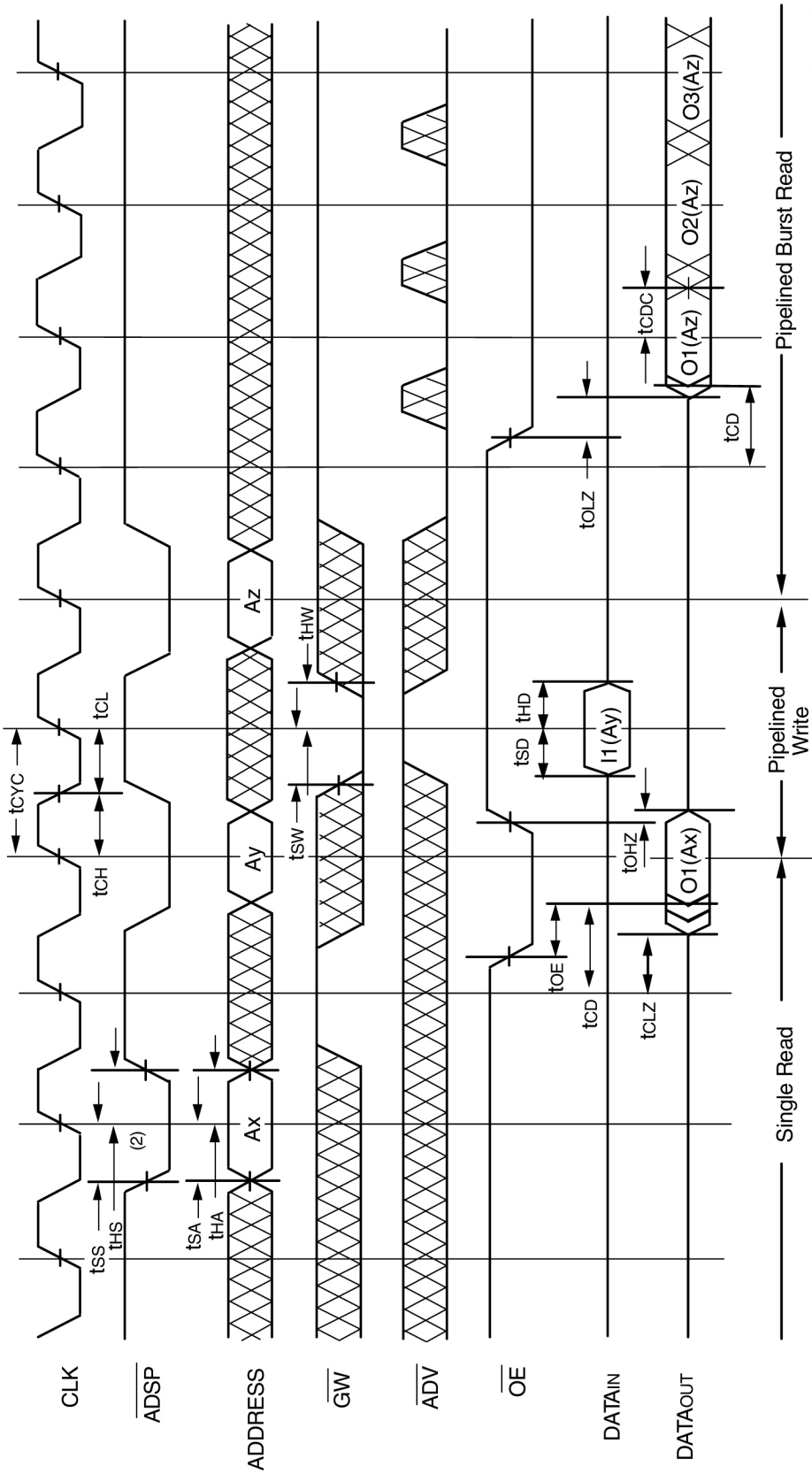
5310 tbl 16

**NOTES:**

1. Measured as HIGH above V<sub>IH</sub> and LOW below V<sub>IL</sub>.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t<sub>CFG</sub> is the minimum time required to configure the device based on the  $\overline{\text{LB0}}$  input.  $\overline{\text{LB0}}$  is a static input and must not change during normal operation.



# Timing Waveform of Combined Pipelined Read and Write Cycles<sup>(1,2,3)</sup>

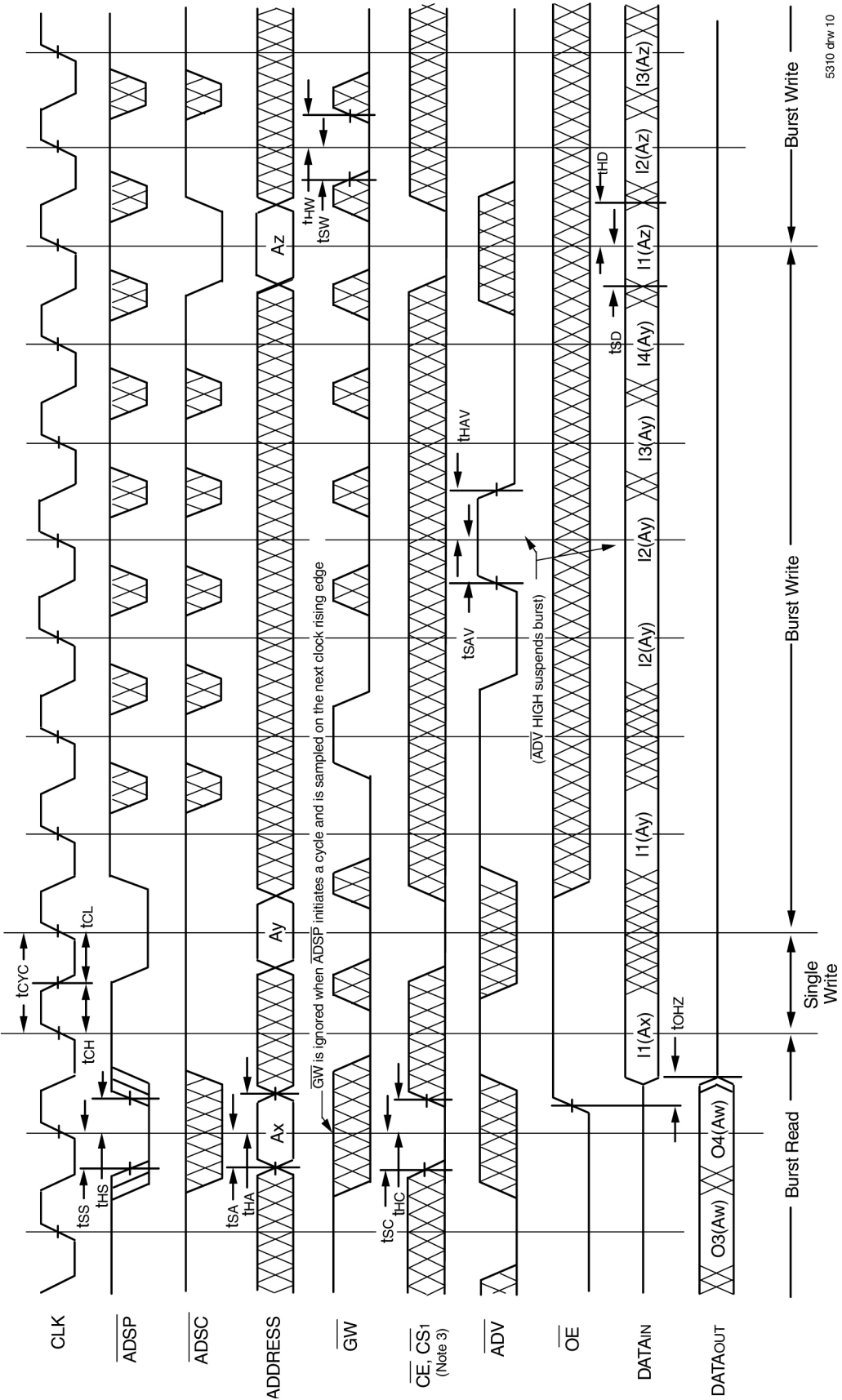


5310 dnv 09

**NOTES:**

1. Device is selected through entire cycle;  $\overline{CE}$  and  $\overline{CS1}$  are LOW,  $\overline{CS0}$  is HIGH.
2. ZZ input is LOW and  $\overline{LBO}$  is Don't Care for this cycle.
3. O1 (Ax) represents the first output from the external address Ax. 11 (Ay) represents the first output from the external address Ay. O1 (Az) represents the first output from the external address Az; O2 (Az) represents the next output data in the burst sequence of the base address Az, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the  $\overline{LBO}$  input.

# Timing Waveform of Write Cycle No. 1 — $\overline{\text{GW}}$ Controlled<sup>(1,2,3)</sup>

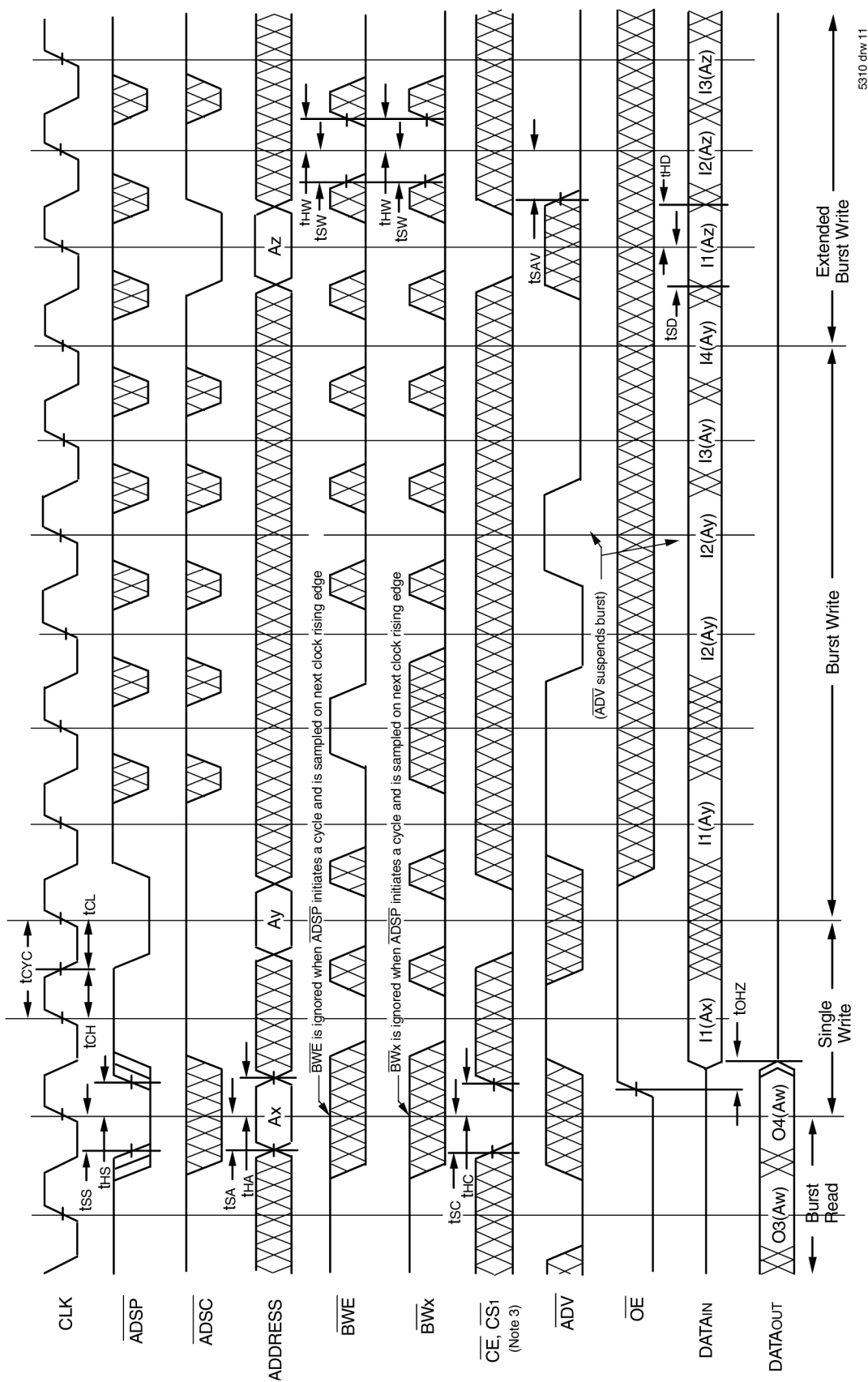


5310 drw 10

**NOTES:**

1. Z<sub>Z</sub> input is LOW,  $\overline{\text{BWE}}$  is HIGH and  $\overline{\text{LBO}}$  is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the  $\overline{\text{LBO}}$  input. In the case of input I2 (Ay) this data is valid for two cycles because  $\overline{\text{ADV}}$  is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the  $\overline{\text{CE}}$  and  $\overline{\text{CS1}}$  signals. For example, when  $\overline{\text{CE}}$  and  $\overline{\text{CS1}}$  are LOW on this waveform, CS0 is HIGH.

# Timing Waveform of Write Cycle No. 2 — Byte Controlled<sup>(1,2,3)</sup>

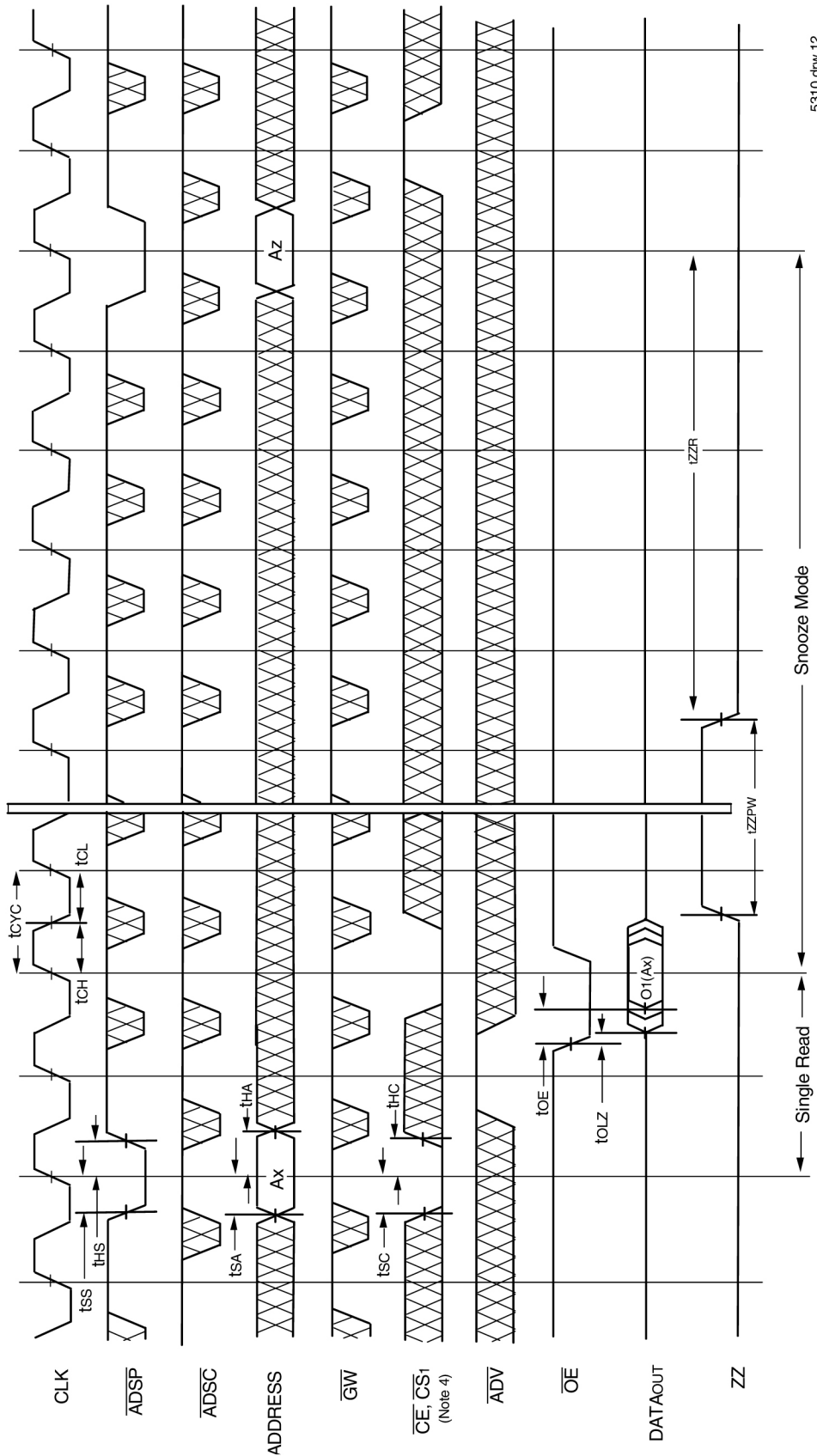


5310 drw 11

**NOTES:**

1. Zz input is LOW,  $\overline{GW}$  is HIGH and  $\overline{LBO}$  is Don't Care for this cycle.
2.  $O4(Aw)$  represents the final output data in the burst sequence of the base address  $Aw$ .  $I1(Ax)$  represents the first input from the external address  $Ax$ .  $I1(Ay)$  represents the first input from the external address  $Ay$ ;  $I2(Ay)$  represents the next input data in the burst sequence of the base address  $Ay$ , etc. where  $A0$  and  $A1$  are advancing for the four word burst in the sequence defined by the state of the  $\overline{LBO}$  input. In the case of input  $I2(Ay)$  this data is valid for two cycles because  $\overline{ADV}$  is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the  $\overline{CE}$  and  $\overline{CS1}$  signals. For example, when  $\overline{CE}$  and  $\overline{CS1}$  are LOW on this waveform,  $\overline{CS0}$  is HIGH.

# Timing Waveform of Sleep (ZZ) and Power-Down Modes<sup>(1,2,3)</sup>

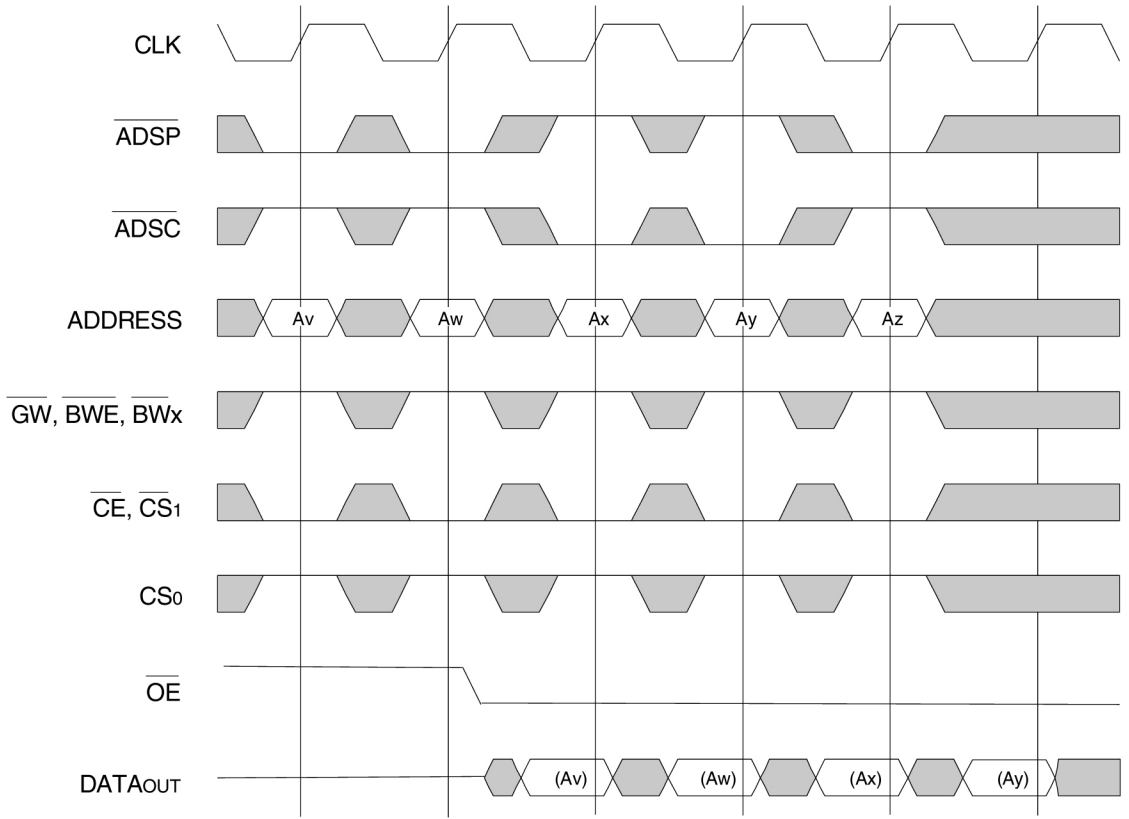


5310 drw 12

**NOTES:**

1. Device must power up in deselected Mode
2. LBO is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS0 timing transitions are identical but inverted to the CE and CS1 signals. For example, when CE and CS1 are LOW on this waveform, CS0 is HIGH.

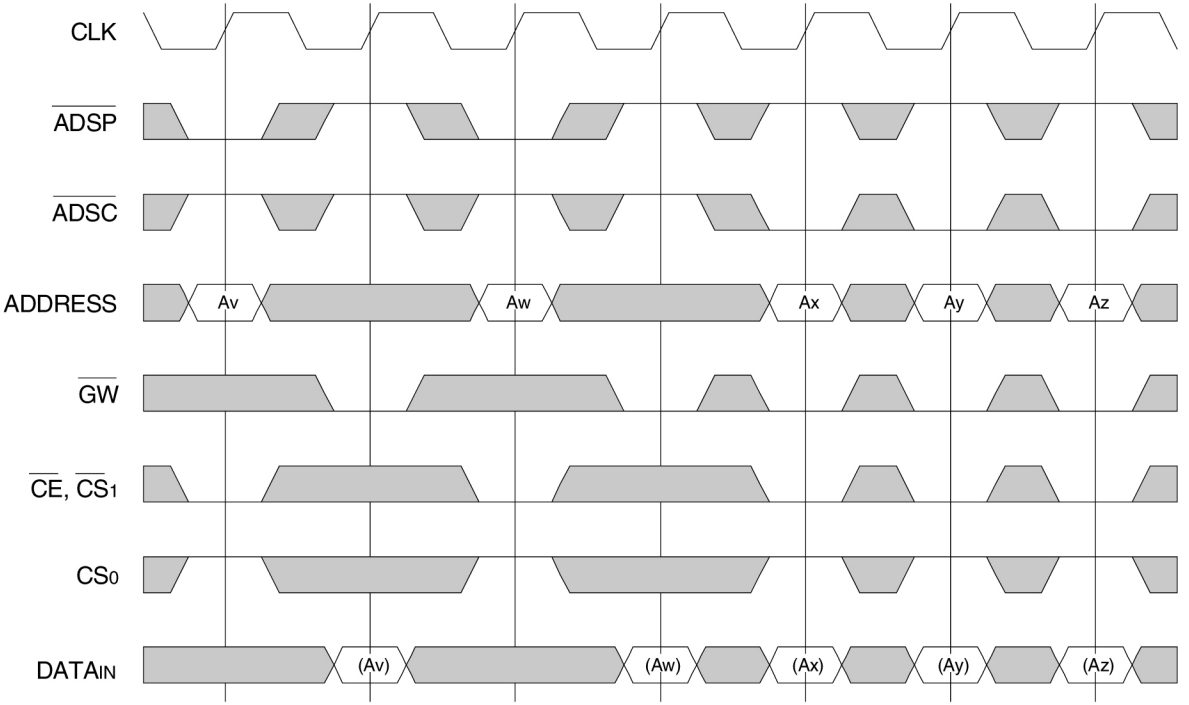
# Non-Burst Read Cycle Timing Waveform



- NOTES:**
1. ZZ input is LOW,  $\overline{ADV}$  is HIGH and  $\overline{LBO}$  is Don't Care for this cycle.
  2. (Ax) represents the data for address Ax, etc.
  3. For read cycles,  $\overline{ADSP}$  and  $\overline{ADSC}$  function identically and are therefore interchangeable.

5310 dnr 14

# Non-Burst Write Cycle Timing Waveform

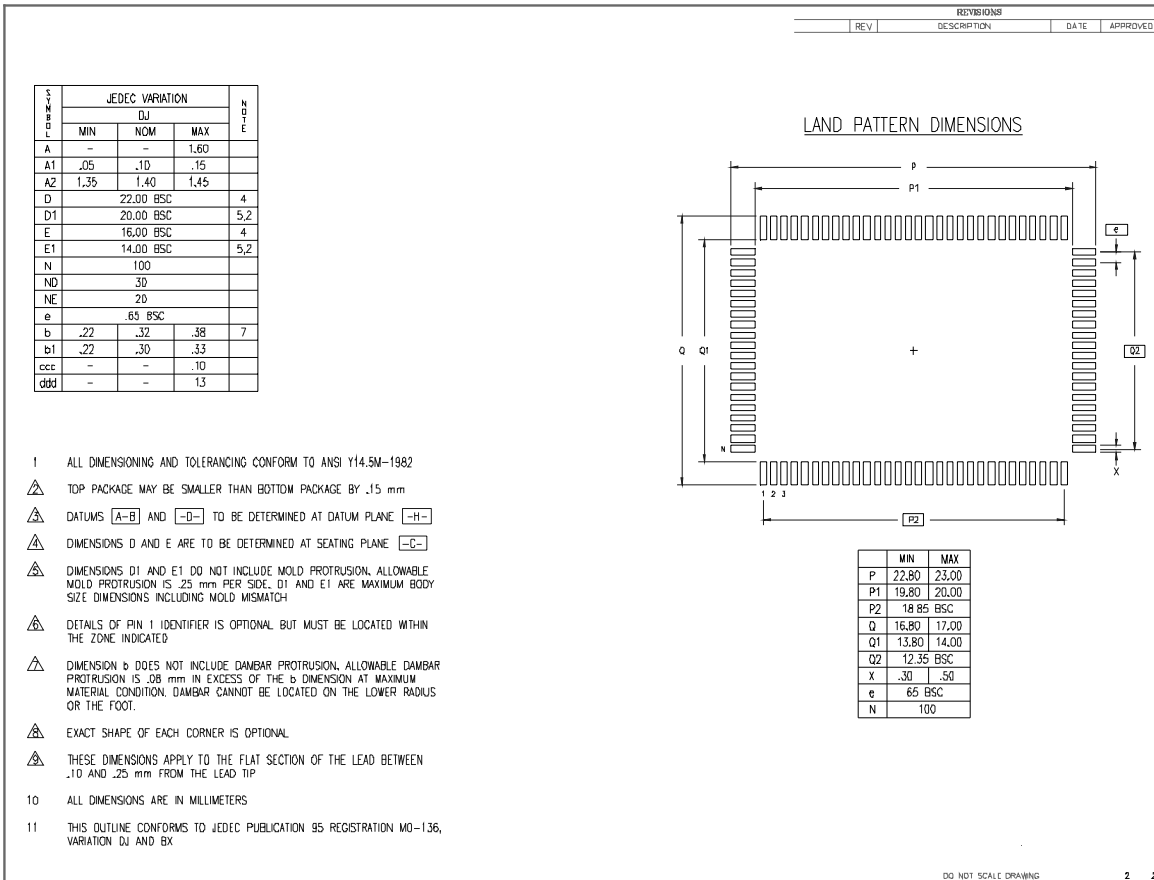
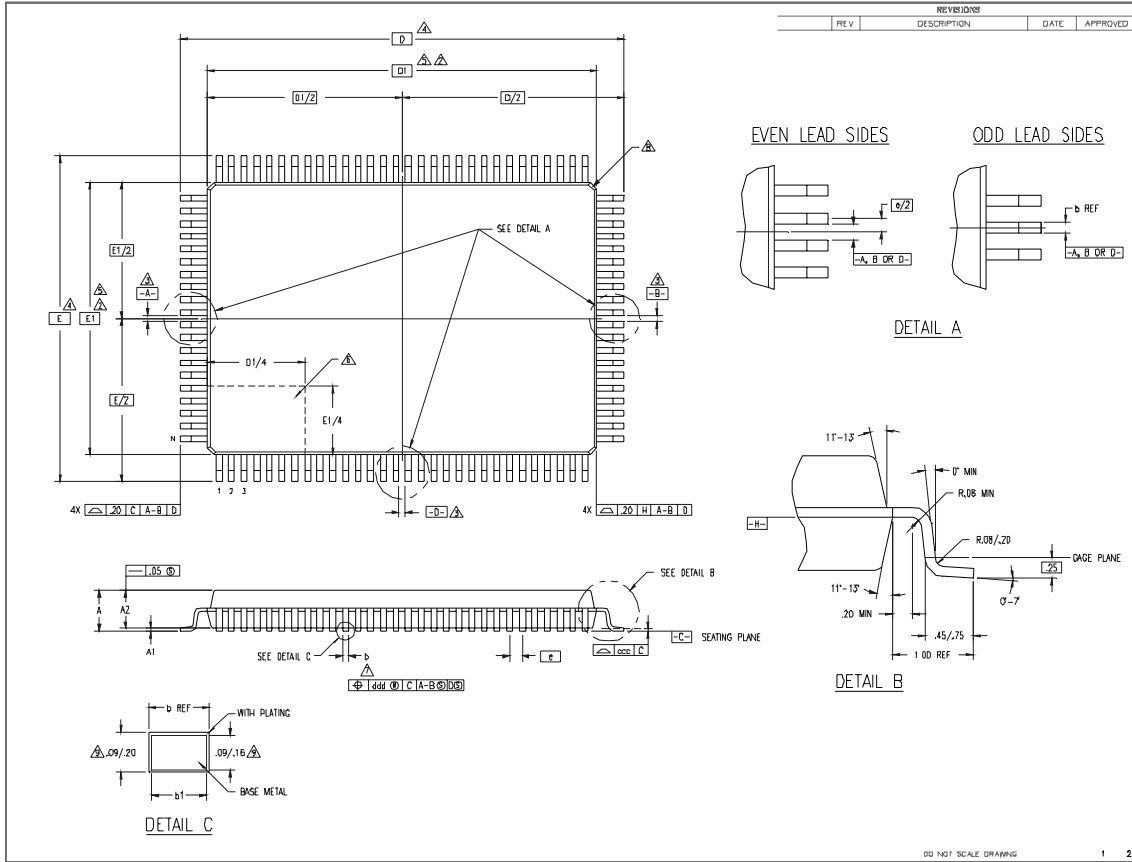


- NOTES:**
1. ZZ input is LOW,  $\overline{ADV}$  and  $\overline{OE}$  are HIGH, and  $\overline{LBO}$  is Don't Care for this cycle.
  2. (Ax) represents the data for address Ax, etc.
  3. Although only  $\overline{GW}$  writes are shown, the functionality of  $\overline{BWE}$  and  $\overline{BWx}$  together is the same as  $\overline{GW}$ .
  4. For write cycles,  $\overline{ADSP}$  and  $\overline{ADSC}$  have different limitations.

5310 dnr 15



# 100-Pin Plastic Thin Quad Flatpack (TQFP) Package Diagram Outline

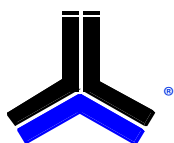


## ORDERING INFORMATION

Alliance	Organization	VCC Range	Package	Operating Temp	Speed Mhz
AS8C803600-QC150N	256K x 36	3.1 - 3.4V	100 pin TQFP	Comercial: 0 - 70C	150
AS8C801800-QC150N	512K x 18	3.1 - 3.4V	100 pin TQFP	Comercial: 0 - 70C	150

## PART NUMBERING SYSTEM

AS8C	Device	Conf.	Mode	Package	Operating Temp	Speed	N
Sync. SRAM prefix	80 = 8M	18= x18 36 = x36	01= ZBT 00 = Pipelined 25 = Flow- Thru	Q = 100 Pin TQFP	0 ~ 70C	150MHz	N= Leadfree



Alliance Memory, Inc.  
551 Taylor way, suite#1,  
San Carlos, CA 94070  
Tel: 650-610-6800  
Fax: 650-620-9211

[www.alliancememory.com](http://www.alliancememory.com)

Copyright © Alliance Memory

All Rights Reserved

Part Number: AS8C803600/801800

Document Version: v. 1.0

© Copyright 2003 Alliance Memory, Inc. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at any time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warrantee to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance's Terms and Conditions of Sale. The purchase of products from Alliance does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems implies that the manufacturer assumes all risk of such use and agrees to indemnify Alliance against all claims arising from such use.